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Optimization of Ohmic Contacts and Surface Passivation for 'Buffer-Free' GaN HEMT Technologies

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Abstract

Gallium nitride high electron mobility transistors (GaN HEMTs) draw attention from high frequency and high power industries due to unique properties including high electron mobility and saturation velocity combined with high breakdown voltage. This makes GaN HEMTs suitable for power devices with high switching speed and high frequency applications with high power density requirements. However, the device performance is still partly limited by problems associated with the formation of low resistivity ohmic contact, trapping effects, and the confinement of the two-dimensional electron gas (2DEG).

In this work, reproducible deeply recessed Ta-based ohmic contacts with a low contact resistance of 0.2 - 0.3 Ωmm, a low annealing temperature of 550 - 600 °C, and a large process window were optimized. Low annealing temperature reduces the risk of 2DEG degradation and promotes better morphology of the ohmic contacts. Deeply recessed ohmic contacts beyond the barrier layers make the process less sensitive to the etching depth since the ohmic contacts are formed on the sidewall of the recess. The concept of deeply recessed low resistivity ohmic contacts is also successfully demonstrated on different epi-structures with different barrier designs.

Passivation with silicon nitride (SiN) is an effective method to suppress electron trapping effects. Low Pressure Chemical Vapor Deposition (LPCVD) of SiN has shown to result in high quality dielectrics with excellent passivation effect. However, the surface traps are not fully removed after passivation due to dangling-bonds and native oxide layer at the interface of passivation and epi-structure. Therefore, a plasma-free in-situ NH_3 pretreatment method before the deposition of the SiN passivation was studied. The samples with the pretreatment present a 38% lower surface-related current collapse and a 50% lower dynamic on-resistance than the samples without the pretreatment. The improved dynamic performance and lower dispersion directly yield a 30% higher output power of (3.4 vs. 2.6 W/mm) and a better power added efficiency (44% vs. 39%) at 3 GHz. Furthermore, it was found that a longer pretreatment duration improves the uniformity of device performance.

Traditionally, decreasing leakage currents in the buffer and improving electron confinement to the 2DEG are achieved by intentional acceptor-like dopants (iron and carbon) in the GaN buffer and back-barrier layer made by a ternary III-nitride material. However, electron trapping effects and thermal resistivity increase due to the dopants and the ternary material, respectively. In this thesis, a novel approach, where a unique epitaxial scheme permits a thickness reduction of the unintentional-doped (UID) GaN layer down to 250 nm, as compared to a normal thickness of 2 µm. In this way, the AlN nucleation layer effectively act as a back-barrier. The approached, named QuanFINE is investigated and benchmarked to a conventional epi-structure with a thick Fe-doped-GaN buffer. A 2DEG mobility of 2000 $cm^2/V\text{-}s$ and the 2DEG concentration of $1.1 \cdot 10^{13}$ cm^{-2} on QuanFINE indicate that the 2DEG properties are not sacrificed with a thin UID-GaN layer. Thanks to the thin UID-GaN layer of QuanFINE, trapping effects are reduced. Comparable output power of 4.1 W/mm and a PAE of 40% at 3 GHz of both QuanFINE and conventional Fe-doped thick GaN buffer sample are measured.

Keywords: GaN HEMT, ohmic contact, passivation, pretreatment, QuanFINE.

List of Publications

Appended papers

[A] Y.K. Lin, J. Bergsten, H. Leong, A. Malmros, J.T. Chen, D.Y. Chen, O. Kordina, H. Zirath, E.Y. Chang, and N. Rorsman, "A versatile low low-resistance ohmic contact process with ohmic recess and low low-temperature annealing for GaN HEMTs", Semiconductor Science and Technology, Vol. 33, Num. 9, Aug. 2018.

[B] D.Y. Chen, K.H. Wen, M. Thorsell, O. Kordina, J.T. Chen, and N. Rorsman, "Impact of GaN HEMTs performance by in-situ NH_3 pretreatment before LPCVD SiNx deposition", Manuscript.

[C] D.Y. Chen, A. Malmros, M. Thorsell, H. Hjelmgren, O. Kordina, J.T. Chen, and N. Rorsman, "Microwave Performance of 'Buffer-Free' GaN-on-SiC High Electron Mobility Transistors" IEEE Electron Device Letters, Vol. 41, Issue 6, Page 828-831, Apr. 2020.

List of Papers

[D] J. Bremer, D.Y. Chen, A. Malko, M. Madel, N. Rorsman, S. E Gunnarsson, K. Andersson, T. MJ Nilsson, P. E Raad, P. L Komarov, T. L Sandy, M. Thorsell, "Electric-Based Thermal Characterization of GaN Technologies Affected by Trapping Effects" IEEE Transactions on Electron Devices, Vol. 67, Issue 5, Page 1952-1958, Apr. 2020.

Contents

Chapter 1

Introduction

III-nitride semiconductors have demonstrated excellent performance in RF and power applications partially due to their material properties. GaN has a larger bandgap (3.4 eV) compared to more conventional semiconductors such as Si (1.1 eV), SiGe (1.12 eV), InP (1.34 eV), and GaAs (1.42 eV). A large bandgap effectively reduces the thermally-generated carriers and the radiation-induced ionization effects, resulting in a good control of the Fermi level, and minimizes the carrier excitation to the conduction band. [1]. Therefore, GaN can operate at higher voltage and maintain good electric performance in high temperature and radiation environment.

GaN high electron mobility transistors (HEMTs) were initially fabricated on AlGaN/GaN heterojunction, where two-dimensional electron gas (2DEG) can be formed within the quantum-well when two different III-nitride materials with different bandgaps are epitaxially grown. Moreover, a high electron concentration can be obtained due to high polarization fields in III-nitride heterostructure. HEMTs on InAlN/GaN and InAlGaN/GaN heterostructures are also been studied as alternatives to the AlGaN/GaN due to less lattice strain and higher electron concentration [1]. High concentration electrons in the quantum-well can move freely with less scattering effects, resulting in high mobility and high saturation velocity. For the GaN HEMTs, a high saturation velocity can contribute to a higher cut off frequency (f_T), resulting in an improved high-frequency operation capability [2]. GaN HEMTs with properties stated above lead to a higher sheet conductivity and in turn a larger saturation current, which transfer to an improved high-power performance. All these properties combined with high thermal conductivity SiC substrates make GaN HEMTs outperform transistors based on Si, SiGe, InP, and GaAs in power amplifiers operating at frequencies up to ~100 GHz for high frequency devices [3]. High-frequency power amplifiers (PAs) are one of the main applications for GaN HEMTs technologies. Compared to the high-frequency PAs made in more conventional technologies, GaN HEMTs generate higher output power density and larger bandwidth for a given output power level [1]. This advantage allows for compact integrated circuit PAs designs ideal for wireless and satellite communication as well as sensor systems (radars).

GaN HEMTs start conquering the territory of existing technology for microwave and mm-wave applications, including 5G networks in telecom, satellite communication, and sensors (e.g. Radars). The increasing demand for improved data capability in infrastructure for wireless communication calls for systems working at higher frequency where more bandwidth is available [4]. Currently, mature GaN HEMT technologies for sub-6 GHz applications have a gate length of

0.25~0.7 μm. Advanced GaN HEMT technologies have a scaled down gate length of 0.03~0.15 μm, which can cover a wider frequency spectrum owing to higher f_T and maximum frequency of oscillation (f_{max}) [5].

In power conversion applications, SiC devices are much more mature. However, GaN heterostructures with much higher mobility compared to SiC and a comparable breakdown performance hold a potential for next-generation power devices with faster switching speed (~MHz), smaller system size, less switching loss, and better efficiency [6]. GaN HEMTs for power applications are not investigated in this thesis.

Despite the advantage of GaN HEMTs, several problems still remain. It is difficult to form ohmic contacts with a low R_c. Reducing the R_c of ohmic contacts minimizes the series resistance at the source and the drain ports of the transistor, resulting in better device performance. One strategy to form ohmic contact is by regrowth of heavily Si-doped GaN, yielding a R_c smaller than 0.1 Ωmm [7]. However, regrowth is complicated and not cost effective, thus not preferred in the industrial mass-production environment. Alternatively, alloyed Ti or Ta-based ohmic contacts have been reported with R_c of 0.1 – 0.4 Ωmm [8-12]. This approach is currently more suitable for commercial purpose. In this work [Paper A], deeply recessed Ta-based ohmic contacts are further optimized in terms of uniformity, recessed side-wall angle, and recessed depth. This work is based on previous studies resulting in low R_c of 0.14 Ωmm, low annealing temperature of ~550 °C, and good edge acuity [11, 12].

Another issue with GaN HEMTs is DC-RF dispersion effects, caused by surface- and buffer-related electron trapping effects, as well as poor thermal dissipation [13, 14][Paper D]. The problem with thermal dissipation is not studied in this thesis. When the electrons fill the surface traps, negative charges are accumulated on the surface and acts as a virtual gate. Since the trapped electrons are not instantaneously released, transient gate bias shifting, and degradation of the drain current are observed [13]. Dielectric layers are commonly used to passivate the unwanted surface trap states. Various ex-situ/in-situ pretreatments have been investigated, including chemical- and plasma-based methods. In-situ methods are preferred due to reduced risk of contamination and oxidation. However, there are no in-situ pretreatment ever reported for LPCVD SiN passivation [15]. Dichlorosilane (DCS), silane, Ammonia (NH_3), and nitrogen gases are commonly used in LPCVD system. NH_3 has been reported to be effective for removing native oxide and recovering the dangling bond on the GaN surface [16]. Therefore, an in-situ NH_3 surface pretreatment process before LPCVD SiN passivation layer deposition is proposed to mitigate the surface-related trapping effects in [Paper B].

Unlike surface-related traps, which can be minimized by passivation layer and surface pretreatment, buffer-related traps require a heterostructure optimization and reduction of unwanted impurities during epitaxial growth. Traditionally, Fe- and C-doped in GaN buffer layers are used to decrease buffer-related leakages [14, 17]. However, electron trapping effects induced by these dopants limit the large-signal performance. A conventional solution to enhance the confinement of the

2DEG is using an AlGaN back-barrier. Though decent confinement can be achieved by the back-barrier, it trades off with trapping and poor heat dissipation properties [18, 19]. QuanFINE, an advanced 'buffer-free' concept without a thick Fe- or C-doped GaN buffer is presented in [Paper C]. It consists of only a 250 nm thin GaN layer (compared to a thickness of 2 µm in standard structure), allowing the AlN nucleation layer to act as a back-barrier to confine the 2DEG and reducing the trapping effect caused by conventional Fe- and C-dopants.

These topics are discussed and investigated in three chapters. In chapter 2, the fundamental knowledge and formation of ohmic contacts are introduced. Different types of ohmic contacts are compared, including metal-based and regrowth ohmic contacts. Ta-based ohmic contacts are further optimized and presented in [Paper A], yielding a low R_c and a large process window. Secondly, different passivation materials and pretreatment are summarized in chapter 3. LPCVD SiN passivation is selected to reduce the surface traps in this work due to the better dielectric properties and low trapping effects. Further reduction of interface traps between LPCVD SiN and epi-structure by in-situ NH_3 pretreatment is demonstrated in [Paper B]. Finally, in chapter 4, the device performance of HEMTs with the improved Ta-ohmic contacts and a pre-treated passivation layer on the 'buffer-free' QuanFINE heterostructure is benchmarked against a conventional Fe-doped thick GaN heterostructure [Paper C].

Chapter 2

Ohmic contacts for GaN HEMTs

2.1 Introduction of ohmic contacts

Good ohmic contacts with a low R_c are essential for transistors operating at high frequency and high power density. Reducing the R_c of ohmic contacts benefits the device with higher output power, better efficiency, and lower noise. However, it is difficult to form ohmic contacts on wide bandgap III-nitrides semiconductor due to the large Schottky barrier at the interface between metal and semiconductor [20]. Compared to intrinsic Si (i-Si) with a smaller bandgap energy of 1.1 eV and smaller energy offset between the conduction band and Fermi level, intrinsic GaN (i-GaN) material has a larger bandgap of 3.4 eV, resulting in an even higher Schottky barrier height (Φ_B) with less thermionic electron transport. Besides, a larger width of the depletion region (W_d) formed by band bending beneath the metal-GaN junction further reduces the probability of electron tunneling (Fig. 2.1).

One strategy to achieve ohmic contacts with a low R_c is to reduce the Schottky barrier height by selecting the metal with a smaller Φ_M such as Ti (4.33 eV) and Ta (~4.0-4.8 eV) [20, 21]. Another solution is to modify the Fermi level in the GaN by intentional Si doping such as regrown contact [7] or Si ion-implantation [10] This results in n-GaN with a smaller depletion region width (shorter tunneling distance) which is inversely proportional to the semiconductor n-type doping concentration (N_d):

$$W_d \propto \frac{1}{\sqrt{N_d}} \qquad (2.2)$$

Nitrogen-vacancies, which act as n-type doping [11, 22], can also be formed during the annealing process of metal ohmic contacts. The ohmic contact metals (Ti, Ta) extract nitrogen from GaN to form TiN and TaN, generating nitrogen vacancies. The Ti-N and Ta-N is reported with a small work function of 3.74 and 4.75 eV, respectively, contributing to a lower Φ_B [23, 24]. However, too much Ti as the bottom layer leads to the formation of the voids below the TiN [22]. The Al layer plays a complex role in Ti- and Ta-based formation of ohmic contacts on AlGaN/GaN heterostructure. Al is commonly utilized in the ohmic metal stacks, in which facilitates a smooth transient of the work function and supports the extraction of nitrogen from GaN as Al-N phase. However, Al in the metal stacks alloys with Ti layer, making Ti lose the reactive ability with GaN [22]. On the other hands, Al in the AlGaN barrier prevents the extraction of N, since the bonding of Al-N is stronger than Ti-N. This protects the 2DEG from degradation during high-temperature processing. Therefore, the thickness ratio between Ti and Al is required to be optimized. However, a drawback associated with Al is that the annealing temperature higher than the melting point of Al (660 °C) usually causes poor surface morphology and edge acuity, which makes the downscaling of source-gate distance for HEMTs difficult.

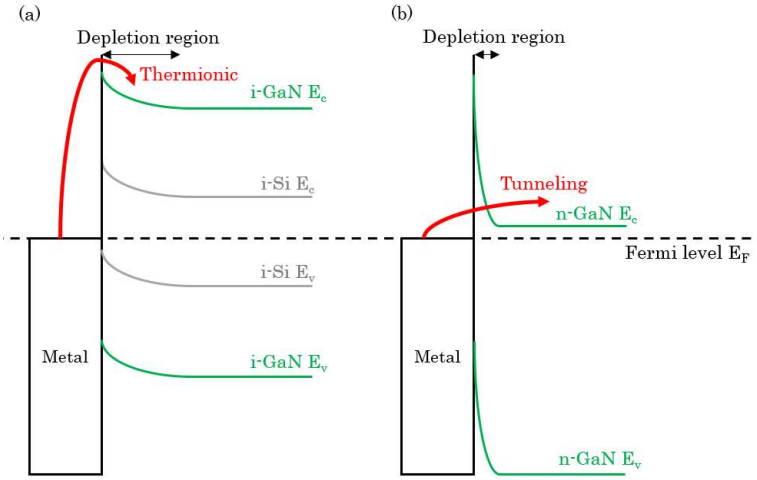

Fig. 2.1. Schottky barriers and band structures of (a) i-GaN and i-Si with thermionic transport dominated, and (b) n-GaN with Tunneling transport dominated.

The transmission line measurement (TLM) is a common method to characterize the electrical properties of ohmic contacts. Using this method, R_c, R_{sh}, specific contact resistance, and transfer length can be readily extracted with good accuracy [25]. A TLM characterization structure (Fig 2.2a) consists of several ohmic contacts, separated by increasing distance (e.g. 5 to 30 µm; denoted as d_1 to d_5). Four-probe measurements with current conducted by two probes and voltage measured by the other two probes are performed to directly eliminate the impact of the resistance in the probe.

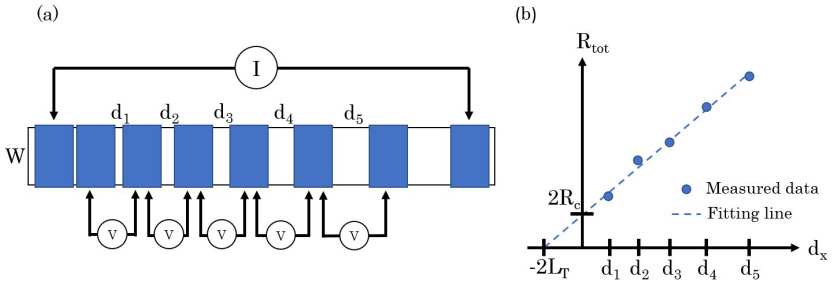

Fig. 2.2. (a) Schematic of TLM structure and (b) extrapolate method of R_c.

The total resistance (R_{tot}) of each spacing is calculated from the measured voltage and current. R_{tot} is the sum of the R_c, the resistance of ohmic metal electrodes (R_m) and semiconductor (R_{semi}):

$$R_{tot} = 2R_m + 2R_c + R_{semi} \tag{2.3}$$

Since the R_m is generally much smaller than R_c, it can be neglected. R_{semi} is the resistance calculated from the R_{sh} of 2DEG:

$$R_{semi} = \frac{R_{sh}}{W} \times d_x \tag{2.4}$$

Through measuring R_{tot} from all spacings on TLM structure, the R_c and R_{sh} can be extracted from Fig.2.2b and Equation 2.3.

The current flow through the semiconductor is uniform. However, the flow into the contacts is exponentially decreasing from the edge of contacts. At the far edge, there is zero current flow, which is known as the current crowding effect. The transfer length (L_T), which can be extracted by TLM measurement (Fig 2.2b) is the average distance that the carrier transport from the semiconductor to the contact. An effective area can be calculated as L_TW. The contact resistivity (ρ_c) can be calculated from:

$$\rho_c = R_c \times L_T W \tag{2.5}$$

2.2 Ohmic process and design

2.2.1 Planar contacts

The fabrication of planar contacts requires lithography, metal deposition, and annealing. In the lithography step, the region for ohmic will be opened, followed by a lift-off process after metal deposition. Inside the opening area, several kinds of pretreatment are reported including wet chemical and plasma pretreatments. Wet chemical treatments including HF, buffered HF, HCl, HNO_3, H_2SO_4, KOH, NaOH, NH_4OH, and $(NH_4)_2S_x$ can minimize the surface carbon or oxygen related contamination [16, 26-30]. Plasma pretreatments including H_2, N_2, O_2 (descum), Cl-based, SF_6, and Ar have been developed to remove the surface native oxide layer, lithography residue, and to recover the surface dangling bond with an improvement

of the surface termination and Ga-N stoichiometry [8]. Besides the surface pretreatment, Si ion-implantation was developed for planar and recessed contacts before the metal deposition to modify the surface i-GaN into the n-GaN, resulting in a shorter tunneling path [10]. However, the activation of the implanted Si requires high-temperature annealing (>1000°C), which tend to degrade the 2DEG, since the epitaxial growth temperature is at a similar range. Ohmic metal stacks are deposited by evaporation or sputtering. Details of the metal stacks design are discussed in section 2.2.3. Annealing of the ohmic metal stacks is then performed in a rapid thermal processing system (RTP) under oxygen-free ambient. Normally, Ar or N_2 are used as ambient gases during the high-temperature process.

The formation of planar ohmic contacts with low R_c might suffer from issues of reproducibility and uniformity, due to different barrier design and thickness. Generally speaking, a thicker barrier increases the tunneling distance between the metal and 2DEG. A higher Al content in the AlGaN barrier increases the barrier height, resulting in low thermionic transport probability. Sometimes, a thin AlN exclusion (spacer) layer is inserted between the barrier layer and the 2DEG to further confine the 2DEG. This thin layer can cause an even more difficult situation of forming ohmic contacts with low R_c. These reasons motivate the need for alternative approaches including the regrown contacts and deeply recessed contacts [Paper A].

2.2.2 Recessed contacts

Though the annealing in planar contacts makes the barrier act as an n-type semiconductor by generating the nitrogen vacancies in the AlGaN/GaN barrier, the distance is still long for the electrons to effectively tunnel to the 2DEG. Shallow recessed contacts have been developed to minimize the tunneling distance by etching the barrier of the epi-structure by Cl-based dry etching by inductively coupled plasma-reactive ion etching (ICP-RIE). A thinner barrier results in a shorter tunneling distance between metal and 2DEG (Fig. 2.3a). However, the reduction of the barrier thickness also reduces the 2DEG concentration, leading to an insufficient carrier density for a high level of tunneling transportation. Therefore, the trade-off between the barrier thickness and the 2DEG density requires a new method to obtain contacts with lower R_c. Some reports indicate that the optimized etching depth is 1~5nm above the 2DEG [9, 12, 31]. However, commercially available ICP-RIE cannot provide a uniform and repeatable etching depth over a full wafer. Due to this problem, deeply recessed contacts, which etch through the GaN region that contains 2DEG, were developed in [Paper A] (Fig. 2.3b) (section 2.3). Deeply recessed contact is less sensitive to the etching depth since the contact region is formed at the recessed sidewall.

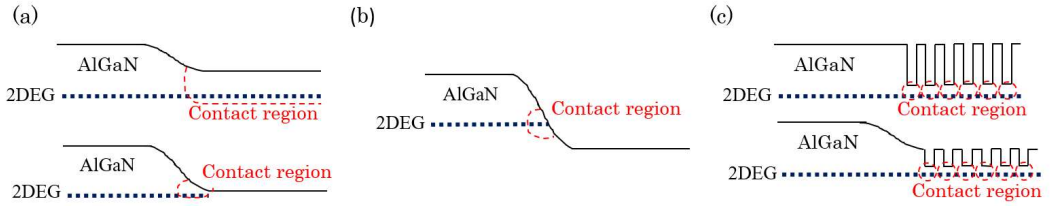

Fig. 2.3. (a) shallow recessed contacts and a trade-off between etching depth and 2DEG density, (b) deeply recessed contacts, and (c) patterned recessed contacts [9].

An alternative solution to prevent the decrease of 2DEG density due to a thinner barrier is patterned recessed contacts. The size of the via hole pattern is big enough for the metal to reach the bottom during deposition; and also small enough to prevent the impact of 2DEG density, resulting in a low R_c of 0.12 Ωmm by Ti-based metal stacks [9].

Regrown contacts have been developed by combining the strategy of recess etching and high Si n-type doping. It delivers extremely low R_c (<0.1 Ωmm) as compared to conventional alloyed ohmic contacts (R_c >0.1 Ωmm) since n-GaN with high concentrate Si-dopants is lattice-match regrown by either molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) in the recessed area, providing both large amount of electrons and the minimized tunnelling distance between the semiconductor and contact metal on top of the regrown n-GaN [7, 32].

2.2.3 Contact metal designs

Metal stacks need to fulfill the two requirements to form good ohmic contacts with low R_c, including a low work function of the first (bottom) metal layer and a capability of extracting nitrogen from GaN. Several reported contacts are summarized in Table 2.1.

Table 2.1. OHMIC CONTACTS EXAMPLES REPORTED IN LITERATURE.

	Metal stacks	$Al_xGa_{1-x}N$ barrier [x], [nm]	AlN exclusion layer [nm]	Anneal temperature [°C]	R_c [Ωmm]	Contact categories	Ref	Year
A	Ti/Al/Ni/ Au	26%, 18	0	825	0.18	Planar contact	[33]	2013
B	Ti/Al/Ni/ Au	30%, 25	0	830	0.1	Planar contact with plasma treatment	[8]	2018
C	Ti/Al/Ni/ Au	30%, 24	1	850	0.12	Patterned shallow recessed contact	[9]	2018
D	Ti/Al/Ni/ Au	30%, 27	0	Without anneal	0.4	Recessed, Si ion implantation	[10]	2006
E	Si/Ge/Ti/ Al/Ni/Au	23%, 18	0	820	0.3	Planar contact	[34]	2017
F	Ta/Si/Ti/ Al/Ni/Ta	26%, 18	0	850	0.22	Planar contact	[33]	2013
G	Ti/TiN	20%, 20	2	850	0.13	Planar contact	[35]	2014
H	Ti/TiN	35%, 20	0	850	0.6	Planar contact	[35]	2014
I	Ti/Al/Ti/ TiN	25%, 20	1	550	0.21	Shallow recessed contact	[31]	2018
J	Ti/Al/W	26.4%, 23	0	500	0.35	Planar contact	[36]	2018
K	Ti/Al/Ni/ TiN	23%, 19	1	830	1.1	Planar contact	[37]	2020

L	Ti_5Al_1/TiN	25%, 20	0	880	0.06	Planar contact	[38]	2020
M	Ta/Al/Ta	25%, 25	0	575	0.28	Planar contact	[11]	2011
N	Ta/Al/Ta	14%, 22	0	550	0.06	Planar contact	[11]	2011
O	Ta/Al/Ta	30%, 15	0	550-600	0.21/0.27	Shallow recessed contact	[39]	2015
P	Ta/Al/Ta	25%, 20	0	575	0.24	Deeply recessed contact	[Paper A]	2018
Q	Ta/Al/Ta	25%, 19	1	575	0.21	Deeply recessed contact	[Paper A]	2018
R	Ta/Al/Ta	30%, 11	1	575	0.25	Deeply recessed contact	[Paper A]	2018
S	--	25%, 22	0	Without anneal	0.2	MBE regrown contact	[40]	2011
T	Ti/Au	InAlN/GaN	0	Without anneal	0.05	MBE regrown contact	[7]	2020
U	--	--	0	Without anneal	0.1	MOCVD regrown contact	[32]	2020

Conventional Ti/Al/Ni/Au contacts are presented in example A-C. It is generally easier to obtain ohmic contacts with a low R_c on epi-structures without an AlN exclusion layer. Example B presents an example, as opposed to A, demonstrating the need for proper surface pretreatments before the metal deposition by removing the surface oxide and contamination. Example C shows a robust low R_c by patterning the recessed ohmic contact. Without completely removing the barrier layer, the 2DEG is preserved and the tunneling distance is also reduced by the recessed pit-hole.

Example D-F demonstrate the conventional Ti/Al-based metal schemes with Si, which is an n-type dopant for GaN. However, Si with a high work function of 4.85 eV generates a large Φ_B [41], leading to less possibility of thermionic transport at the metal-semiconductor interface. Example F deposits the Si on top of the small work function Ta layer, resulting in a lower R_c than for example D and E.

Al is an essential component in ohmic contacts since it supports the extraction of the nitrogen from GaN, forming Ti-Al-N or Al-N phase alloy. However, the surface morphology and the edge acuity are poor. The Al is proposed to be removed or using the TiN and W as a cap layer to improve the edge acuity for a downscaled device as presented in examples G-K. A recent report (example L) also claims that Ti and Al deposited as an alloy instead of separated layers provide better ohmic contact with lower R_c than standard multilayer stacks.

Unlike conventional metal stacks ohmic contacts, annealing is not required for regrown contacts (examples S-U) since the barrier is completely removed by dry etching, and the heavily Si-doped n-type GaN is lattice-matched regrown by MBE or MOCVD within the recessed region, resulting in smaller Φ_B and shorter tunneling distance. R_c smaller than 0.1 Ωmm is reported on different epi-structures. Regrown contacts on InAlN barrier, which has a higher 2DEG concentration than the conventional AlGaN barrier, provide an extremely low R_c of 0.05 Ωmm [7].

2.3 Deeply recessed Ta based ohmic contacts

Ti-based metal stacks are normally selected as ohmic contacts for GaN HEMTs. However, the high annealing temperature of Ti/Al contact leads to poor-quality

surface and edge. Ta/Al/Ta ohmic contacts with a low annealing temperature (<600 °C) have been developed to overcome the above issues. Examples M and N present Ta/Al/Ta planar contacts with a low R_c of 0.28 and 0.06 Ωmm, respectively. A lower R_c is achieved on the epi-structure with a thinner and lower Al content AlGaN barrier. Although an AlGaN barrier with higher Al content generates a higher 2DEG concentration, it is difficult to form the ohmic contacts with low R_c due to higher barrier height. An approach of shallowed recessed Ta/Al/Ta contacts is performed in example O, which delivered a lower R_c than that of the planar Ta/Al/Ta contacts on a higher Al content AlGaN barrier epi-structure.

In this work, deeply recessed Ta/Al/Ta ohmic contacts with low annealing temperature are proposed to minimize the impact of etching depth by directly contacting the recessed sidewall [Paper A]. Several fabrication conditions, including metal coverage, recessed sidewall angle, the thickness of contact metal, and different barrier epitaxial designs are investigated to achieve optimized ohmic contacts.

The TLM structure (Fig. 2.2a) for ohmic contact characterization is fabricated through the following procedures. The AlGaN/GaN on SiC epi-structure is cleaned by standard RCA cleaning to remove surface organic and metallic contaminants followed by the deposition of SiN passivation layer by low-pressure chemical vapor deposition (LPCVD). The active area of TLM is isolated by mesa dry etching. The ohmic contacts lithography is performed by mask-free laser writing (Heidelberg Instruments DWL 2000), enabling the control of the photoresist profile by the dose of exposure. The recessed etching is performed by ICP-RIE followed by diluted HF and HCl dipping, Ta/Al/Ta metal deposition, lift-off process in acetone, and the annealing process by RTP in N_2 ambient.

Due to the deep etching beyond the 2DEG, the contact is formed at the recessed sidewall (Fig. 2.5). Therefore, the impact of the bottom contact Ta metal coverage for the R_c was studied. The experiment was performed by tilting the sample for 10 degrees during the Ta metal deposition by evaporator with the automatic sample rotation. The results (Fig. 2.4) reveal that the sample tilting during deposition is required to repeatably and uniformly achieve ohmic contacts with low R_c.

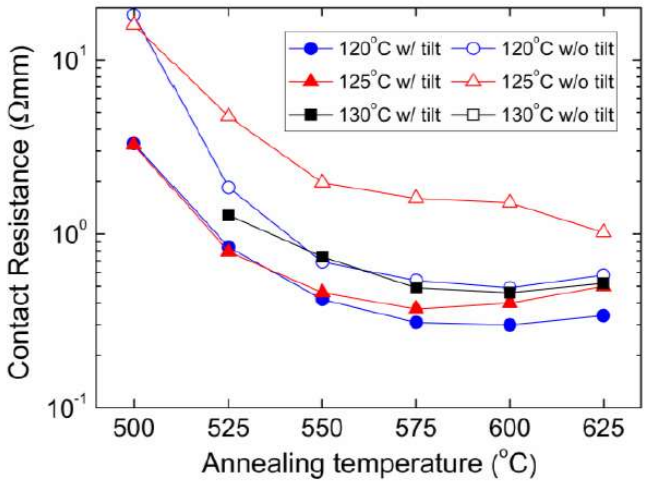

Fig. 2.4. The impact of R_c by sample tilting during metal deposition [Paper A].

The angle (θ in Fig. 2.5) of the recessed sidewall is another parameter that strongly impacts the formation of deeply recessed ohmic contacts since the 2DEG properties at the sidewall is influenced by the thickness of AlGaN barrier. A smaller recessed sidewall angle reduces the 2DEG density but benefits from shorter tunneling paths and better metal coverage, and vice versa. Therefore, the optimization of θ is performed by controlling the photoresist profile with reversal baking and exposure dose setting. A steeper profile leads to a larger θ due to the weaker shadowing effect, resulting in an enhancement of anisotropic etching. The optimized θ is around 55°, achieved with a reversal baking temperature of 125 °C with the exposure dose of 85.6 mJ/cm², yielding a deeply recessed ohmic contact with a R_c smaller than 0.3 Ωmm.

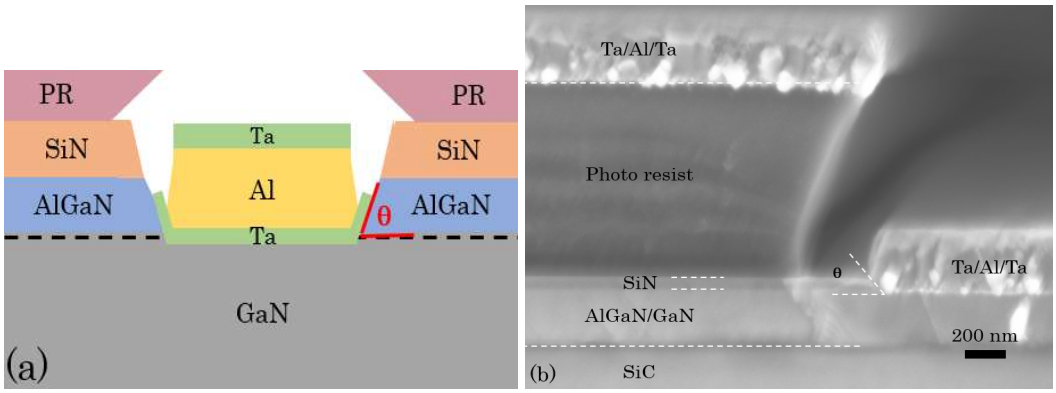

Fig. 2.5. (a) The schematic [Paper A] and (b) the SEM image of the deeply recessed Ta/Al/Ta ohmic contacts.

The donor-like nitrogen vacancies in GaN have been reported to be generated by the extraction procedure from Ta and Al, resulting in Ta-N, Al-N, and Ta-Al-N phases. The exact thickness of the bottom contact metal layer is one of the major parameters of forming the ohmic contact with low R_c. Different Ta deposition

thickness is studied including 5, 10, 15, 20, and 30 nm, yielding 3, 7, 11, 16, and 26 nm Ta thickness on the recess sidewall, respectively. The best R_c of 0.24 Ωmm was achieved for the samples annealed at 575 °C for 26 minutes with 20 nm bottom Ta-layer thickness [Paper A].

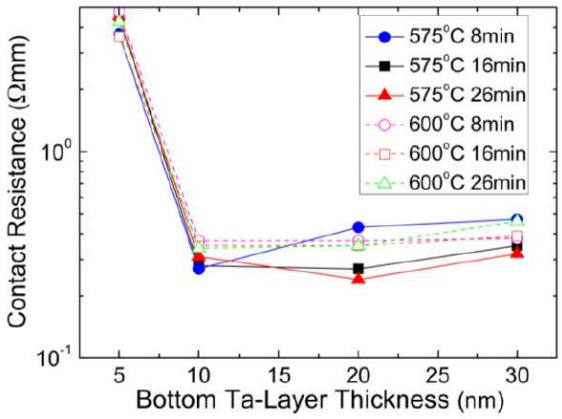

Fig. 2.6. Contact resistance depends on the bottom Ta contact metal thickness and annealing temperature [Paper A].

The last test verified the deeply recessed Ta/Al/Ta ohmic contacts on different epi-structures including the Epi I (20 nm $Al_{0.25}Ga_{0.75}N$ / GaN), Epi II (19 nm $Al_{0.25}Ga_{0.75}N$ / 1 nm AlN_{ex} / GaN), and Epi III (2 nm GaN_{cap} / 11 nm $Al_{0.3}Ga_{0.7}N$ / 1 nm AlN_{ex} / GaN). A 20 nm Ta is evaporated with tilting for the bottom contact layer. The characterization results (Table 2.2) indicate that ohmic contacts with a R_c smaller than 0.25 Ωmm can be formed on all epi-structures with a recess depth of more than 10 nm beyond the 2DEG. Overall, all samples present good ohmic contacts although the etching depth is different, revealing that the processing window is sufficiently large for sidewall contact type ohmic contacts.

Table 2.2. SUMMARY OF TLM RESULTS ON DIFFERENT EPI-STRUCTURES [PAPER A]

Epitaxial structure	Etching depth (nm)	Contact resistance (Ω·mm)
I	$t_{barrier}$ + 10	0.24
	$t_{barrier}$ + 25	0.33
II	$t_{barrier}$ + 10	0.21
	$t_{barrier}$ + 20	0.36
III	$t_{barrier}$ + 10	0.25
	$t_{barrier}$ + 15	0.25

Chapter 3

Passivation and surface pretreatment for GaN HEMTs

3.1 Introduction of passivation layer

Passivation dielectric is an important part of AlGaN/GaN HEMTs to reduce the surface-related trapping effects, minimize the surface leakage currents, sustain the device breakdown characteristics, and protect the surface from ambient moisture and oxygen. Many different passivation methods and materials have been studied to find compatible and robust passivation dielectrics for HEMTs including SiN_x, SiO_x, and SiO_xN_y deposited by plasma-enhanced chemical vapor deposition (PECVD), Si_xN_y by reactive sputtering, Al_2O_3, AlN, HfO_2, SiO_2 by atomic layer deposition (ALD), and Si_xN_y by LPCVD. Other methods including catalytic chemical vapor deposition (CVD), electron-cyclotron CVD, remote plasma CVD, and in-situ MOCVD are also reported for the passivation of the AlGaN/GaN HEMTs.

The most important role of the passivation layer is to suppress electron trapping at the surface. When a heterostructure is grown, defects such as pits are found on the surface. Several reports have indicated that the surface defects might be originated from threading dislocations [42, 43]. Native oxide is another trap state that is commonly created after the exposure to ambient air. The trapped electrons act as a virtual gate on the surface, which depletes channel electrons and increases the on-resistance [44]. The passivation is either removing the surface oxide and minimizing the surface defects [45], or increasing the amount of positive charges at the passivation/epi-structure interface, which neutralizes the AlGaN polarization charges, which results in the decrease of the surface-related depletion of the 2DEG [46].

Trapping effect characterization

Unwanted traps lead to current dispersion, knee walk-out, and degradation of dynamic R_{on}. Pulsed-IV characterization is a technique that can characterize the trapping effects. Gate and drain voltage pulses are then applied from a quiescent point (pinch-off condition, $V_{GS} < V_{TH}$) to an active point (on-condition, $V_{GS} > V_{TH}$), while the drain current is measured (Fig 3.1). The pinch-off condition for the quiescent point enables a nearly thermal-free characterization.

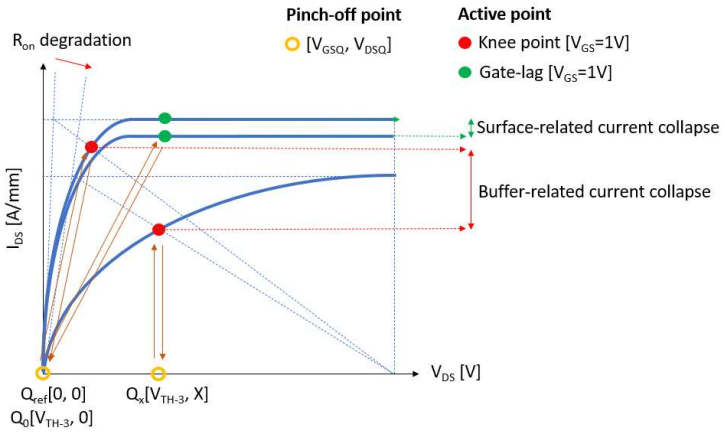

Figure 3.1. Trapping effect characterization method

To characterize the surface-related traps, the quiescent bias points (V_{GSQ}, V_{DSQ}) of (0, 0) and (V_{TH-3}, 0), denoted as Q_{ref} and Q_0, respectively, are applied on HEMTs. V_{DSQ} is set at 0 V to prevent the activation of the buffer-related traps. The surface-related current collapse which is also known as gate-lag is defined as:

$$Z_{gate-lag}\ [\%] = \left|\frac{I_{DS}(Q_0) - I_{DS}(Q_{ref})}{I_{DS}(Q_{ref})}\right| \cdot 100 \qquad (3.1)$$

When the drain voltage is applied for quiescent biases under pinch-off condition, (V_{GSQ}, V_{DSQ}) of (V_{TH-3}, X), denoted as Q_X ,the traps states in the buffer will be filled, resulting in knee walk-out, current collapse, and degradation of dynamic R_{on}, commonly defined as drain-lag:

$$Z_{drain-lag}\ [\%] = \left|\frac{I_{DS}(Q_X) - I_{DS}(Q_{ref})}{I_{DS}(Q_{ref})}\right| \cdot 100 \qquad (3.2)$$

3.1.1 PECVD Si_xN_y, SiO_2, and SiO_xN_y passivation

PECVD is commonly selected for the deposition of the passivation layer on the AlGaN/GaN HEMTs. SiN_x, SiO_x, and SiO_xN_y have been reported as promising dielectric materials to suppress the surface trapping effects and leakage, and

improve the breakdown characteristics (summarized in section 3.15) [47]. The reaction processes for the SiN_x using either N_2 or NH_3 are:

$$SiH_x + NH_x \rightarrow SiN_x + (H_2) \quad (3.3)$$

$$SiH_x + N \rightarrow SiN_x + (H_2) \quad (3.4)$$

While the reaction process for SiO_x is:

$$SiH_x + N_2O \rightarrow SiO_x + (H_2 + N_2) \quad (3.5)$$

A combination process (equation 3.3 and 3.5) can create a SiO_xN_y passivation layer:

$$SiH_x + N_2O + NH_3 \rightarrow SiO_xN_y + (H_2 + N_2) \quad (3.6)$$

The passivation dielectrics are deposited at a temperature of 200~400 °C, which is very suitable for post-processing passivation layer and gate dielectric due to low temperature with a minimized impact for the device.

The SiN_x and SiO_x deposited by the PECVD are strongly influenced by the precursor flow rates and ratio, the RF power, the chamber pressure, and the deposition temperature. The impact of the deposited dielectrics from these parameters are summarized (Table 3.1 and 3.2). Generally speaking, higher SiH_4 flow and higher SiH_4:NH_3 ratio lead to a faster deposition rate with a higher refractive index since the growth of SiN_x is controlled by SiH_4. With a higher RF power, the deposition rate of the dielectric film increases with a lower refractive index and more compressive stress, due to an enhancement of aminosilane (an intermediate product of SiN, $Si(NH_2)_4$) formation [48].

Table 3.1. IMPACT OF PECVD SiN_x DEPOSITION BY PROCESSING PARAMETERS

SiN_x	Deposition rate	Refractive index	Film stress
↑ SiH_4 flow	↑	↑	more compress
↑ NH_3: SiH_4 ratio	↓	↓	more tensile
↑ RF power	↑	↓	more compress
↑ Temperature	↓	--	more tensile

Table 3.2. IMPACT OF PECVD SiO_x DEPOSITION BY PROCESSING PARAMETERS

SiO_x	Deposition rate	Refractive index	Film stress
↑ SiH_4 flow	↑	↑	more tensile
↑ N_2O: SiH_4 ratio	↓	↓	--
↑ RF power	↑	↓	more compress
↑ Temperature	↑	↑	--

3.1.3 ALD Al_2O_3, AlN, HfO_2, SiO_2 passivation

Different dielectrics deposited by Atomic layer deposition (ALD) such as Al_2O_3, AlN, HfAlO, and SiO_2 have been reported as a passivation layer on AlGaN/GaN HEMTs with promising coverage and reduction of surface-related trapping effects (details given in section 3.1.5). ALD deposits the thin film layer by layer on the target substrate. Each precursor chemical carries different elements of the target thin-film material to the surface (known as chemisorption), separated by the evacuation purge process in between, resulting in a monolayer of the thin film (~1Å) on the substrate. An ALD cycle time for a monolayer thin film is several seconds with a process temperature of 200~500 °C, which is also suitable for post passivation like the PECVD. One significant advantage of ALD is conformality of the surface deposition with the same thickness irrespective of the surface morphology and defects. This processing advantage makes ALD suitable not only for the surface passivation but also for the coating on the recessed etching sidewall and the bottom of the trenches. Moreover, the covalent bonding of the ALD process passivation layer provides good adhesion to the target surface.

3.1.4 LPCVD SiN_x passivation

LPCVD can be categorized into two different systems including a hot wall and a cold wall system. The advantage of a cold wall system is that it reduces the material deposited on the wall of the chamber, reducing the fall of particles on the sample and minimize the memory effects of the materials. On the other hand, the hot wall system has an advantage of high throughput. The formation of SiN_x in LPCVD is a chemical reaction of dichlorosilane (DCS, $SiCl_2H_2$) and ammonia (NH_3) under high temperature (700~800 °C) and low chamber pressure (<500 mTorr). Though the typical deposition rate is low (~10 nm/minute), several wafers can be processed in a single run with excellent uniformity. The process of forming SiN_x (Si_3N_4) is:

$$3SiCl_2H_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2 \quad (3.4)$$

SiN_x deposited by LPCVD has advantages as a passivation layer on AlGaN/GaN HEMTs. The properties of SiN_x deposited under high temperature by LPCVD has less thermal degradation during device operation at high power since the operating temperature (200~300 °C) is much lower than the SiN_x deposition temperature. Moreover, LPCVD SiNx is more suitable for the passivation-first process, which protects the epi-wafer from the beginning of the processing, since it is the first processing step with the highest temperature among other steps.

The deposition parameters of the LPCVD include the precursor flow rates, the ratio between DCS and ammonia, the chamber pressure, and the deposition temperature [49-51]. Increasing the flow rate, chamber pressure, and deposition temperature will increase the deposition rate due to a more effective chemical reaction. The relative ratio between DCS and NH_3 will impact the refractive index and the internal stress of the SiN_x thin film due to different stoichiometric of Si and N in the SiN_x [52].

Table 3.3. IMPACT OF LPCVD SiN_X DEPOSITION BY PROCESSING PARAMETERS

SiN_x	Deposition rate	Refractive index	Film stress
↑ SiH_4 flow	↑	↑	↓ more compress
↑ NH_3: SiH_4 ratio	--	↓	↑ more tensile
↑ Chamber pressure	↑	--	↑ more tensile
↑ Temperature	↑	↑	↓ more compress

3.1.5 Passivation layers on GaN HEMTs

Good passivation needs to fulfill several criteria, including low surface leakage current, low surface-related trapping effects, and high breakdown voltage. However, there are trade-offs between each requirement. Table 3.4 summarizes the advantages and issues of different passivation layer material by different fabrication methods.

Table 3.4. EXAMPLES OF PASSIVATION LAYER REPORTED IN LITERATURES

	Passivation dielectric material	Deposition tool	Epitaxial barrier design	Advantages	Comments	Ref.
A	SiN_x	PECVD	AlGaN	Reduce current collapse Reduce gate lag Improve noise performance	Plasma damage	[53, 54]
B	Bilayer high freq./low freq. SiN_x	PECVD	GaN_{cap}/AlGaN	Reduce plasma damage Reduce R_{on} and dynamic R_{on}	--	[55]
C	SiN_x	PECVD	GaN_{cap}/AlGaN/ AlN_{ex}	Reduce current collapse	Drain leakage	[56, 57]
D	SiO_x	PECVD	GaN_{cap}/AlGaN/ AlN_{ex}	Large bandgap Reduce drain leakage	Trapping is more than PECVD SiN_x	[56, 57]
E	SiO_xN_y	PECVD	GaN_{cap}/AlGaN/ AlN_{ex}	Reduce drain leakage Improve transconductance Improve drain current	Trapping is more than PECVD SiN_x	[56, 57]
F	Al_2O_3	ALD	GaN_{cap}/AlGaN	Large bandgap	Trapping is similar or lower than PECVD SiN_x	[58, 59]
G	HfAlO	ALD	GaN_{cap}/AlGaN	--	Trapping is more than PECVD SiN_x	[58]
H	AlN	ALD	AlGaN	Reduce gate leakage Reduce drain leakage	Trapping is similar or lower than PECVD SiN_x	[60]
I	AlN/SiN_x	ALD/PECVD	GaN_{cap}/AlGaN	Improve transconductance Reduce R_{on} and dynamic R_{on}	--	[61, 62]
J	Al_2O_3/SiO_2	ALD/PECVD	GaN_{cap}/AlGaN	Reduce gate-lag	--	[58]
K	SiN_x	LPCVD	GaN_{cap}/AlGaN/ AlN_{ex}	Improve breakdown voltage Reduce degradation after stress Reduce dynamic R_{on}	--	[63]
L	SiN_x	LPCVD	AlGaN/AlN_{ex}	Reduce lateral surface leakage Reduce gate and drain lag	Vertical leakage	[64]
M	Si-rich SiN_x	LPCVD	GaN_{cap}/AlGaN	Reduce dynamic R_{on}	Drain-gate leakage Schottky gate leakage	[65]
N	N-rich SiN_x	LPCVD	GaN_{cap}/AlGaN	Reduce drain-gate leakage Reduce Schottky gate leakage	Trapping effects	[65]
O	Bilayer Si-rich/N-rich SiN_x	LPCVD	AlGaN	Reduce current collapse Reduce gate leakage	--	[64]
P	Si-rich SiN_x	LPCVD	GaN_{cap}/AlGaN	Reduce current collapse Reduce dynamic R_{on}	With in-situ NH_3 pretreatment	[Paper B]
Q	In-situ SiN_x	MOCVD	AlGaN	Reduce trapping effects Improve radiation tolerance Resistant to electric/thermal stress	--	[66, 67]
R	SiN_x	Sputter	AlGaN	Reduce trapping effects	--	[68]
S	Sc_2O_3	MBE	AlGaN	Reduce trapping effects	--	[69]
T	MgO	MBE	AlGaN	Reduce trapping effects	React with ambient H_2O	[69]

Example A-E are the dielectrics deposited by PECVD. Example A confirms that the surface passivation can effectively reduce surface trapping states as compared to non-passivated epi-structure. However, the plasma damage defects generated by ion bombardment during the deposition limit the reduction of trapping effects. Example B presents a bilayer SiN_x deposited by a high-frequency RF source in the beginning, which can minimize the plasma damage, resulting in a further reduction of dynamic R_{on} degradation. Example C indicates that the passivation has a function of reducing surface traps for the epi-structure with or without surface GaN capping layer. Further reduction of surface traps can be performed by surface pretreatment, which will be discussed in section 3.2. SiO_x and SiO_xN_y are also considered as a passivation layer for a power device, which requires high breakdown voltage, due to a larger bandgap of 8.9 eV and higher resistivity than SiN_x. Though the surface-related leakage current can be minimized, the sample with SiO_x and SiO_xN_y passivation layer suffers from severe current collapse and knee voltage walkout due to poor dielectric/epi interface quality, degrading the device performance ultimately.

Several reports also present the passivation layer deposited by ALD. The dielectric thin film is formed by the plasma-free high-quality layer by layer deposition (example F-H). Dielectrics with oxide as components still suffer from trapping effects similar to PECVD SiN_x. Post high temperature (~800 °C) annealing process for ALD dielectrics such as Al_2O_3 and AlN was proposed to improve the dielectric/epi interface quality, resulting in a lower current collapse. Annealed polycrystalline AlN as the passivation layer improves the 2DEG properties by extra polarization force. Combining ALD AlN with the PECVD SiN_x, AlN/SiN_x exhibits a promising reduction of dynamic degradation performance as a passivation layer.

Compared to PECVD, the LPCVD deposited passivation layer potentially beneficial for the dielectric quality (higher deposition temperature) and less damage on the surface of the epi-structure (plasma-free process). Several advantages such as improving breakdown voltage performance, device reliability, and robustness, and minimizing the trapping effects are confirmed for example K-P. Similar to PECVD grown SiN_x, the Si-rich SiN passivation layer grown by LPCVD reduces the surface-related traps by possibly providing the leakage path for carriers to be de-trapped easier. N-rich SiN passivation layer offers a higher breakdown and lower leakage performance which is suitable for the second passivation layer on top of the Si-rich SiN_x. In this work [Paper B], Si-rich SiN_x is selected because it has been already providing a decent reduction of current dispersion since established. More details about combining LPCVD SiN_x and in-situ surface pretreatment will be given in section 3.3.

Other passivation methods such as MOCVD, reactive sputtering, and MBE have also been reported for depositing the passivation layer. MOCVD SiN_x can be grown in-situ on top of the epi-structure without exposure to ambient moisture and oxygen, which provides an oxygen-free interface with potential reduction of trapping effects [66, 67]. Sputter SiN_x also suffer similar surface plasma damage as PECVD SiN_x [68]. Other types of dielectrics including Sc_2O_3 and MgO fabricated by MBE offer a new opportunity of the passivation layer for AlGaN/GaN HEMTs [69].

3.2 Pretreatment for passivation layer

Dangling bonds (nitrogen-vacancy), plasma damage defects, a native oxide layer, carbon-related contamination have been reported as the main reasons for creating surface leakage paths, and surface trap states. Ex-situ and in-situ surface pretreatments are proposed to mitigate these issues including surface reconstruction and contaminant elimination.

3.2.1 Ex-situ pretreatment

Ex-situ pretreatments are normally performed by wet chemical treatment and plasma treatments. Some reports also present thermal annealing at high temperature with different gas flows. The plasma-based treatment will be given in 3.2.2 due to the overlap of information. Table 3.5 summarizes the functions and reactions of different chemical treatments on AlGaN/GaN HEMTs.

Table 3.5. EXAMPLES OF EX-SITU PRE-TREATMENT REPORTED IN LITERATURES

	Pretreatment	Epitaxial surface	Function	Comments	Ref.
A	HCl	GaN	Remove surface oxide Minor remove surface carbon	Form 3D nucleation point defects Chlorine residual	[16, 26-29]
B	HF	GaN	Remove surface oxide Remove surface carbon	Fluorine residual	[16, 26, 29]
C	Buffered HF	GaN	Remove surface oxide	Fluorine residual	[16]
D	NH_4OH	AlN and GaN	Remove surface oxide	Maintain III-N stoichiometry	[16, 30] [Paper B]
E	$(NH_4)_2S$	GaN	Remove surface oxide Provide defect-free surface Prevent surface re-oxide	Sulfide residual Enhance breakdown	[28, 70, 71]
F	KOH	GaN	Remove surface carbon	High surface roughness	[28]
G	RCA SC1	GaN	Remove organic residual Remove surface particles	Form a thin oxide layer	[72] [Paper B]
H	RCA SC2	GaN	Remove metallic contaminants	Left carbon on the surface Form a thin passivizing layer	[72] [Paper B]
I	Piranha	GaN	Remove hydrocarbons Remove hydroxylates	Provide smooth surface	[26]
J	UV/O_3	GaN and AlN	Remove surface carbon	Grow oxide layer	[16, 29]
K	Annealed with SiH_4	AlN	Remove surface oxide	Si deposition on the surface	[16]
L	Annealed with NH_3	In and GaN	Reconstruct GaN surface	Annealed at 700~900 °C	[16]

Example A presents HCl as a commonly used etchant to remove the surface Ga-O on epi-structure, resulting in a reduction of the yellow luminescence due to the change of surface states. The reduction of unwanted surface states mitigates the surface trapping effects. However, the HCl only shows a minor effect on carbon-related contamination. Besides, the formation of the point defects after the dipping of the GaN in the HCl solution leads to the poor morphology of the following passivation layer. Reports also verify that the chlorine-based residual bonds primary with Ga on the surface (saturated the dangling bond).

HF and Buffered HF are oxide etchants commonly used in Si-industry. It easily removes the surface oxide by the fluorine bonding to the Al and Ga as fluorine residual on the surface. The fluorine residual can either be considered as a pretreatment process to reduce the leakage current or be treated as an unwanted virtual gate, which depletes the 2DEG channel carriers. Compared to the strong acid example A-C, NH_4OH not only provides the capability of removing surface

oxide but also leaves no trace of residuals on the epi-structure, maintaining the GaN and AlN stoichiometry. Unlike NH_4OH, the $(NH_4)_2S$ treatment leaves the sulfide residual on the surface.

Examples with mixed chemicals are provided for example G-I. RCA standard cleaning SC1 (H_2O_2+NH_4OH+H_2O) and SC2 (H_2O_2+HCl+H_2O) can effectively remove the surface organic and metallic contaminants, respectively. In the meantime, a thin oxide layer is formed on the surface to protect the epi from other contaminants. Piranha etchant is a strong oxidizing agent due to the mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2). The report shows that the GaN with piranha treatment, yielding a smooth surface with minimized organic residues, is an ideal surface for deposition of the passivation layer such as ALD Al_2O_3.

Gas-phase ex-situ treatments (examples J-L) on GaN also show promising results compared to chemical solution-based treatments stated above. UV/Ozone can effectively remove the carbon-related residues. However, the oxide layer formed by ozone leads to a severe trapping effect for GaN HEMTs. High-temperature annealing treatments for GaN with SiH_4 and NH_3 are also studied. Though SiH_4 removes surface oxide, the unwanted Si layer might cause surface-related leakage current.

In [Paper B], RCA SC1 and SC2 ex-situ pretreatments are performed to remove organic and metallic residues on the surface of the epi-structure, followed by NH_4OH to minimize the oxide layer generated by the RCA treatments. Instead of ex-situ NH_3 annealing, an in-situ NH_3 pretreatment within LPCVD followed by SiN_x deposition is performed after the NH_4OH dipping (details are given in section 3.3).

3.2.2 In-situ pretreatment

Though the surface of the epi-structure can be cleaned by ex-situ treatments, the re-oxidation and re-contamination are reported during the transport of the materials to the passivation system. Thus, in-situ treatments with similar functions as ex-situ treatments are preferred. In-situ pretreatments before the deposition of the passivation layer are mainly performed by plasma-based methods, within PECVD, PEALD, and reactive sputtering systems. Table 3.6 summarizes the functions of different plasma treatments on AlGaN/GaN HEMTs.

Table 3.6. EXAMPLES OF IN-SITU PRE-TREATMENT REPORTED IN LITERATURES

	Pretreatment	Epitaxial surface	Function	Comments	Ref.
A	Hydrogen plasma (H_2)	AlN	Remove carbon and halogen species Remove surface oxide	Hydrogen diffusion into the barrier Formation of Ga droplets	[13, 16, 73]
B	Ammonia plasma (NH_3)	AlGaN and GaN	Remove surface oxide Remove surface carbon	Hydrogen diffusion into the barrier Improve reliability Reduce current collapse	[73, 74]
C	Nitrogen plasma (N_2)	GaN	Remove surface oxide Remove surface fluorine Recover surface nitrogen-vacancy	Reduce surface leakage current Reduce virtual gate behavior Reduce degradation of dynamic R_{on}	[13, 15, 75, 76]
D	Fluorine plasma (NF_3, CF_4, SF_6)	AlGaN and GaN	Modify surface energy states Remove surface oxide	Virtual gate with lower drain current Lower V_{TH} hysteresis Faster surface de-trapping	[77-80]
E	NH_3 gas flow	GaN	Remove surface oxide Reconstruct GaN	Reduce surface-related traps	[Paper B]

Four types of plasma-related in-situ pretreatments have been investigated in the literature to improve the quality of the interface between the passivation layer and the surface of the epi-structure by removing surface oxide and unwanted residues without exposing to the atmosphere before passivation. Hydrogen plasma can effectively remove surface carbon residues and the oxide layer. However, it will react with GaN, generating nitrogen vacancies, due to the formation of Ga-H bonds. Moreover, the reaction of hydrogen with GaN leads to the degradation of HEMTs under the hot electron stress condition [13, 16, 73]. Similar to hydrogen plasma, hydrogen ions in ammonia plasma can diffuse into the barrier, causing similar degradation as hydrogen plasma, though it has nitrogen radicals to recover the stoichiometry of GaN [73, 74]. Pure nitrogen plasma pretreatment shows the most promising results including removing surface native oxide, carbon-related contaminations, and fluorine residues, leading to the reduction of current collapse and the minimizing of leakage path [13, 15, 75, 76]. Fluorine-based plasma shows different effects for HEMTs. A normally-off device with a positive shift of pinch-off voltage can be achieved by fluorine-based plasma pretreatment. On the other hand, the fluorine residues on the surface are considered as extra donor states (virtual gate behavior), leading to the depletion of the 2DEG channel of normally-on devices [77-80].

3.3 In-situ NH_3 pretreatment for LPCVD SiN passivation layer

An effective plasma-free in-situ NH_3 pretreatment before LPCVD SiN passivation on the GaN HEMTs is demonstrated in this work. Ex-situ wet chemical treatments by RCA SC1, RCA SC2, and NH_4OH are selected (fewer side effects) to remove the epi-structure's surface organic, metallic contaminations, and minimize the thickness of surface oxide, respectively, before loading into LPCVD chamber for in-situ NH_3 pretreatment and SiN_x deposition.

3.3.1 Trapping effects and large-signal characterization

Pulsed-IV measurements are performed with a pulse width of 1 µs and a duty cycle of 0.001 % on GaN HEMTs with different in-situ NH_3 pretreatment time. HEMTs on the sample without in-situ NH_3 pretreatment exhibits a higher $Z_{gate\text{-}lag}$ of 16% as compared to that on NH_3 pretreated samples with the $Z_{gate\text{-}lag}$ of 10 % (Fig. 3.2). This result indicates that the in-situ NH_3 pretreatment before the LPCVD SiN_x deposition effectively passivates the surface dangling bonds, resulting in less surface-related trapping.

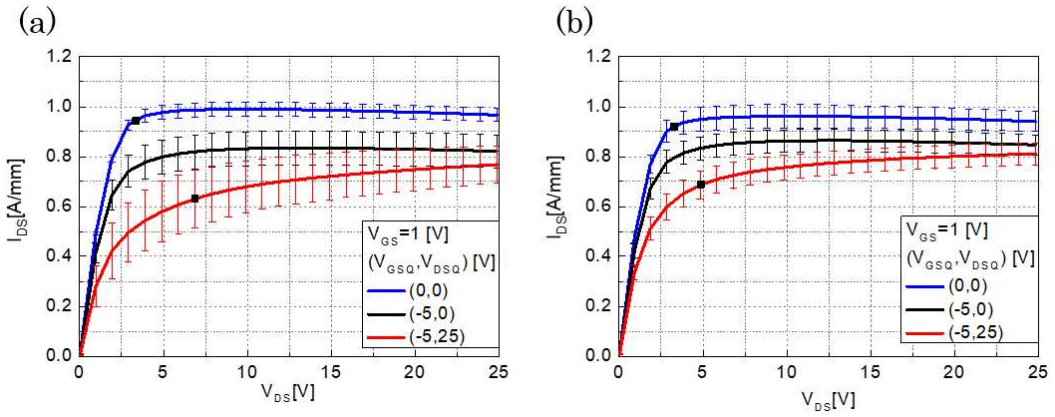

Figure 3.2. Pulsed-IV measurements on 12 randomly selected HEMTs (L_g=200 nm) on the sample with different NH_3 pre-treatment time, (a) 0 min, and (b) 10 minutes [Paper B].

Consistently, pretreated samples also present a 50 % lower dynamic R_{on} compared to that of the untreated sample. A better on-wafer uniformity is also demonstrated in the pre-treated sample as seen in the smaller spread in Fig. 3.2b. The reduction of current collapse and knee walkout directly translate to a higher output power of 3.3 W/mm as compared to the untreated sample with 2.6 W/mm at 3 GHz at 30 V on the device with the L_g of 200 nm (Figure 3.3).

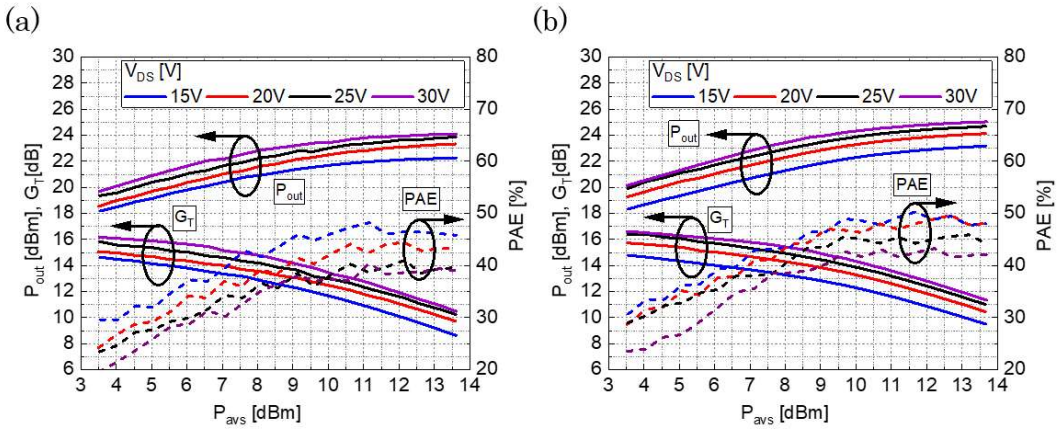

Figure 3.3. Active load-pull measurements at 3 GHz on HEMTs with different NH_3 pretreatment time, (a) 0 min, and (b) 10 minutes [Paper B].

Chapter 4

QuanFINE - a 'buffer-free' heterostructure GaN HEMTs

4.1 Introduction of conventional heterostructure

Conventional AlGaN/GaN HEMTs on SiC heterostructure consists of an AlN nucleation layer (to provide a wetting layer for GaN to dimensionally nucleate), a thick GaN buffer (further improve the GaN crystal quality until reaching good quality in the 2DEG region), and AlGaN barrier (Fig 4.1a). Ideally, the GaN should be grown without impurities as i-GaN. However, the elements and contaminants from chamber in MOCVD will diffuse during the epitaxial growth, acting as unintentional n-type dopants (Si and O) in GaN, resulting in n-GaN behavior. Moreover, massive amounts of defects at the bottom of the GaN buffer with poor crystal quality are also reported, which leads to buffer-related leakage issue. Intentional acceptor-like doping (Fe and C) and band structure engineering (double heterostructures) methods are therefore proposed to compensate the n-type dopants as a semi-insulating GaN buffer and to confine the 2DEG, respectively.

Short channel effects

A reduction of gate length and an increase of drain bias might cause short channel effects, which is a phenomenon where electrons are accelerated by the strong electric field, passing underneath the depletion region formed by the reverse gate bias. With a shorter gate length, the gate capability of depleting the channel is weaker. This fact leads to the reduction of load-line swing, limiting the output power and efficiency of HEMTs. Though the short channel effects can be minimized by reducing the thickness of the barrier layer, tunneling leakage current between

the gate and 2DEG channel might appear. Further improvement of 2DEG confinement and reduction of buffer leakage are presented in the following sections.

4.1.1 2DEG confined by intentional acceptor-like doping

- **Fe-doped GaN buffer**

GaN HEMTs with Fe-doped GaN buffer is commonly used for microwave applications. Compared to C-doping in GaN, Fe-doped GaN HEMTs demonstrate a faster drain current recovery speed (de-trapping around ~10^{-3} sec after turning on the device [17]), which is more suitable for high-frequency operation. A maximum Fe-doping concentration of ~1.3×10^{19} cm^{-3} can be used to achieve semi-insulating GaN buffer without degradation of crystal properties and surface morphology [81, 82]. However, unlike C-doping, the doping memory effect of Fe during the epitaxial growth makes it impossible to achieve a sharp interface between high Fe-doped and low Fe-doped region, resulting in a slow reduction in the Fe concentration after turning off the Fe precursor. Normally, a thickness of 500~1000 nm GaN buffer is required for the Fe doping to decrease the doping from 10^{18} to 10^{16} cm^{-3} (potentially causing Fe contamination in the 2DEG and AlGaN barrier) [17, 83]. Except for this drawback, the p^- n^- junction is not able to be formed between the Fe-doped region and the 2DEG region since the energy level of Fe is 0.7 eV below the conduction band [84]. This advantage allows the trapped-electrons in acceptor-like Fe to be de-trapped back to the 2DEG channel.

Several GaN HEMTs on Fe-doped GaN buffer are reported with an excellent performance at a different frequency. At 4GHz, AlGaN/GaN HEMTs (L_g=0.55 μm)with double field plates have an output power (P_{out}) of 41 W/mm and power added efficiency (PAE) of 60% [85]. At 14 GHz, AlGaN/GaN HEMTs (L_g=0.25 μm) with source-connected field plates have an output power (P_{out}) of 5.2 W/mm and power added efficiency (PAE) of 57.4 % [86]. At 40 GHz, a 4×45 μm AlGaN/GaN HEMTs (L_g=0.1 μm) with a thin UID GaN channel on Fe-dope thick buffer exhibit a P_{out} of 2 W/mm and a superior PAE of 35 % [87].

Because of the well-controlled and high-maturity growth, a Fe-doped GaN buffer heterostructure with standard AlGaN barrier was chosen as a reference epi-structure to study the impact of in-situ NH_3 pretreatment for LPCVD SiN_x passivation layer on GaN HEMTs [Paper B] and to benchmark the high-frequency device performance of the advanced QuanFINE heterostructure [Paper C].

- **C-doped GaN buffer**

Carbon is another dopant that commonly been used to compensate for the unwanted impurities and contaminants during GaN epitaxial growth to achieve semi-insulating GaN buffer. Moreover, a higher resistivity can be provided by C-dopants due to a deeper energy state of ~0.9 eV as compared to that on Fe-dopants, resulting in a higher breakdown voltage behavior, which is particularly suitable for high voltage applications [14]. However, a reverse bias p^--n^- junction might be formed between the holes (high concentration C-related traps with 0.9 eV above

valence-band) and 2DEG, leading to a trade-off of more severe current collapse and the degradation of dynamic R_{on} than Fe-doped buffer since the procedure of the de-trapping from C-doped region back to 2DEG is limited by the diode-like P-N junction [88]. Therefore, different carbon doping profiles in heterostructure have been studied and optimized to achieve decent 2DEG confinement, high breakdown voltage, and lower trapping effects.

Unlike Fe-doped buffer, which suffers from the growth memory effects and the poor controllability of doping profile, a rapid modification of the C-doping concentration can be achieved (Fig. 4.1). Normally, the carbon concentration is controlled by growth conditions including temperature, pressure, the ratio of III-V precursors, and the carrier gas. Lower growing temperature and lower chamber pressure lead to an increase of C-dopants concentration in GaN. A higher flow rate of Ga-precursor (trimethylgallium, TMGa) leads to the reduction of C-doping concentration. On the other hand, a higher carbon concentration requires a lower NH_3 flow rate. Moreover, the carrier gas (H_2) within MOCVD also influence the concentration of C-dopants in the heterostructure [89]. Though carbon doping can easily be modified by growth parameters, the material properties including GaN crystal quality, point defects, surface morphology might be compromised. Other C-doping methods include adding a carbon precursor with the mixture of Ga and nitrogen precursors during CVD growth or using hydrocarbon-based precursors such as propane was realized, which allows unaffected of GaN crystal quality and performs the compensation of unintentional background impurities dopants [88, 90].

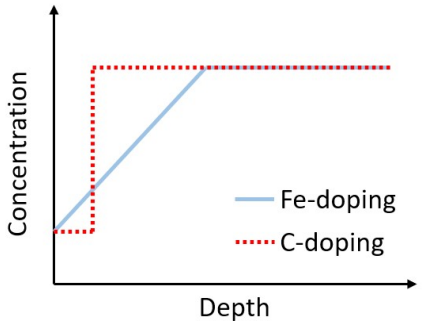

Figure 4.1. Fe-doping and C-doping profile.

Generally, carbon can bond with Ga or N. Carbon is found to be an acceptor when substituted for nitrogen (C_N) and a shallow donor when substituted for gallium (C_{Ga}). Based on yellow luminescence experiments, C_N is well accepted as a deep acceptor with the ionization energy of 0.9 eV [14]. Moreover, the interstitial carbon can also be formed in wurtzite GaN, being a deep donor in *p*-type GaN and a deep acceptor in *n*-type GaN [91].

Though C-doped GaN is reported with deeper trap state and trapping issues, decent high-frequency performance can be achieved by proper optimization of the C-doping profile. S. Gustafsson et al. demonstrated an improvement of the C-doping

profiles with high/low and stepped C-doping concentration. Lower leakage current of 10^{-4} A/mm, lower current collapse dynamic R_{on}, and high output power of 2.3 W/mm and high drain efficiency of ~45 % at 3 GHz can be achieved on optimized stepped C-doping epi-structure [92]. A 2×50 μm AlGaN/GaN HEMTs (L_g=0.11 μm) with a thin UID GaN channel on C-dope thick GaN buffer exhibits a P_{out} of 3.8 W/mm and a PAE of 48 % at 40 GHz [93].

4.1.2 2DEG confined by band structure engineering

In addition to intentional doping can improve the confinement of the 2DEG in the channel, band structure engineering by a back-barrier is an alternative method to confine the 2DEG (Fig. 4.2). Similar to the conventional barrier, the back-barrier provides a larger barrier height beneath the 2DEG, which can effectively confine the 2DEG in the quantum well from the backside as a sandwich-like heterostructure (so-called double-heterostructure). Due to the epitaxial growth availability and the requirement of band structure offset, AlGaN and InGaN are commonly employed as back-barrier materials. Enhanced confinement in the double heterostructure makes it suitable for the HEMTs with short gate lengths (L_g < 150 nm). However, AlGaN shows higher thermal resistance compared to GaN and AlN, resulting in degradation of device performance and reliability due to phonon scattering and poor crystal quality when it is used as a back barrier [94]. Moreover, defects, and dislocations, considered as trap center, in the AlGaN back-barrier are revealed by buffer-related trapping effects characteristics (drain-lag measurement) [18, 19]. According to the issues stated above, double heterostructure is more suitable for low voltage operation to minimize the impact of buffer related traps in the back-barrier. R. Pecheux, et al. demonstrated HEMT with the gate length of 220 nm on AlN/GaN/$Al_{0.08}Ga_{0.92}N$ double heterostructure, exhibiting an output power of 2.3 W/mm and PAE of 37 % at V_{DS} of 10 V operating at 40 GHz thanks to the good confinement of AlGaN back-barrier [95]. Another back-barrier material is InGaN which has better thermal conductivity than AlGaN was reported beneath lattice-matched InAlN/GaN HEMTs with a record cut-off frequency of 300 GHz for the gate length of 30 nm device and no sign of short channel effects for the device with the gate length of 70 nm [96]. However, the temperature mismatch between the InGaN back barrier and the GaN channel is large, which hinders the maturity of using InGaN as a back barrier in GaN HEMTs.

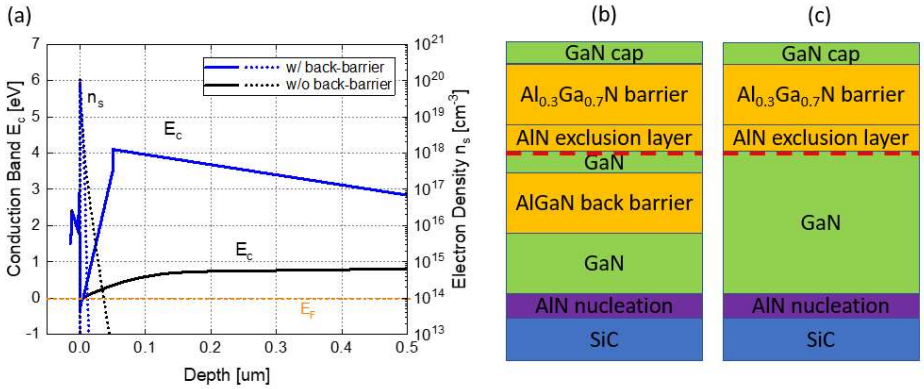

Figure 4.2. (a) TCAD simulation of the conduction band (E_c) and electron density (n_s) for heterostructure (b) with and (c) without AlGaN back-barrier.

4.2 QuanFINE - a buffer-free concept

One possible method to minimize the trapping effects without sacrificing the 2DEG confinement is a high crystal quality thin UID-GaN layer sandwiched in between the top barrier (i.e. AlGaN barrier in this study) and the bottom AlN nucleation layer. Since the UID-GaN layer is sufficiently thin, the AlN nucleation layer can act as the back-barrier, resulting in a double heterostructure (Fig. 4.3).

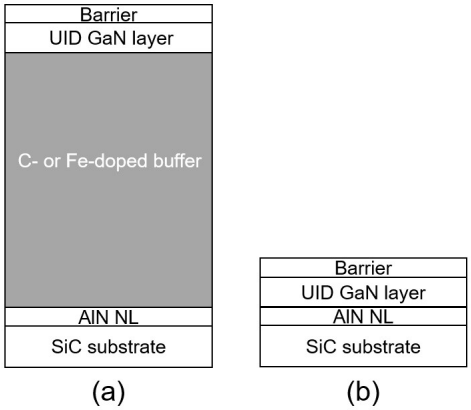

Figure 4.3. The concept of (a) conventional thick intentional-doped GaN buffer and (b) 'buffer-free' QuanFINE epi-structures [Paper C].

The simulation result (Synopsys Sentaurus TCAD) of QuanFINE and conventional thick Fe-doped GaN buffer is presented in Fig. 4.4. The band diagram and the distribution of the electron concentration show that QuanFINE heterostructure potentially offers a better 2DEG confinement than a conventional Fe-doped buffer.

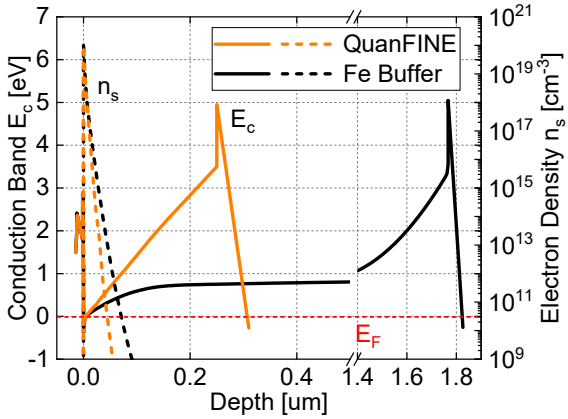

Figure 4.4. Conduction band (E_c) (Line) and electron density (n_s) (dashed line) of QuanFINE and "Fe buffer" at the V_{DS} of 0 V [Paper C].

Previous attempts with a thin GaN layer present a poor 2DEG performance due to high dislocation density, which degrades the electron mobility. In this work, a high-quality thin UID-GaN layer is enabled to be grown by a transmorphic epitaxial growth of the AlN nucleation layer on the SiC substrate. It is achieved by out-of-plane compositional-gradient with an in-plane vacancy-ordering interface growth method which consists AlN nucleation layer, $(Al_{2/3}Si_{1/3})_{1-x}N$, $(Al_{1/3}Si_{2/3})_{2/3+x}N$, and the SiC substrate. Al from precursor and Si from SiC react with N, forming the first layer on the SiC substrate ($(Al_{1/3}Si_{2/3})_{2/3+x}N$). The rest of the Si further reacts with Al and N precursors ($(Al_{2/3}Si_{1/3})_{1-x}N$). After the Si from SiC is fully consumed, AlN nucleation layer starts growing [97]. Moreover, the AlN nucleation layer grown with transmorphic epitaxy has a low thermal boundary resistance, enabling good thermal dissipation capability [97, 98] [Paper D]. From contactless Lehighton measurement, excellent 2DEG properties with a 2DEG concentration of $1.16 \cdot 10^{13}$ cm^{-2} and electron mobility of 2030 $cm^2/V \cdot s$ are obtained, which indicate no compromise in the crystal quality of QuanFINE by significantly reducing UID-GaN layer thickness.

4.3 Benchmark QuanFINE to conventional Fe-doped heterostructure

To fully examine the potential and fairly benchmark of QuanFINE, HEMTs on QuanFINE are compared to a Fe-doped epi-wafer from Cree Inc. (denoted "Fe Buffer") with identical device processing flows and nominally the same top barrier design, which consists a 2 nm GaN cap, 10 nm $Al_{0.3}Ga_{0.7}N$ barrier, and 1 nm AlN exclusion layer (AlN_{ex}). Beneath the 2DEG, QuanFINE has a 250 nm thick UID-GaN layer grown on a 60 nm AlN nucleation layer on top of the SiC substrate; "Fe Buffer" epi-wafer has an 1800 nm thick Fe-doped GaN buffer grown on an AlN nucleation layer on SiC substrate.

The HEMTs processing starts from the ex-situ surface chemical cleaning by RCA SC1, SC2, and diluted ammonia dipping to remove the surface organic, metallic,

and particle containments followed by in-situ NH_3 pretreatment before SiN passivation layer deposited by LPCVD with a thickness of 60 nm [Paper B]. The mesa isolation is performed by a dry etching process with a depth of 165 nm into the HEMT structure. The deeply recessed low annealing temperature gold-free Ta/Al/Ta ohmic contacts are applied for source and drain electrodes on QuanFINE and "Fe buffer" with a contact resistance of 0.32 Ωmm and 0.28 Ωmm, respectively [Paper A]. HEMTs with an L_g of 200 (100) nm, which have a source-drain distance of 2.75 (1.75) µm, and a gate-drain distance of 1.75 (0.95) µm, and a drain-side field plate of 0.25 (0.15) µm, were fabricated. The total gate width of the HEMTs characterized in this study is 2×50 µm. The device is fabricated as simple as possible (Fig 4.5) to minimize any uncertainty from extra passivation layer or field plates, which might lead to the difficulty of analyzing the results.

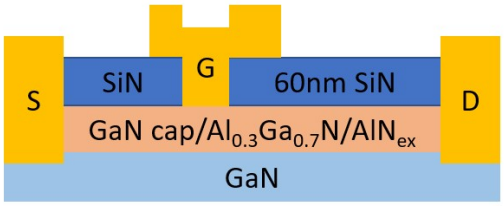

Figure 4.5. Schematic of HEMTs layout.

The 2DEG properties were characterized after the device processing on van der Pauw structures. The electron densities are $1.02 \cdot 10^{13}$ cm^{-2} and $1.08 \cdot 10^{13}$ cm^{-2}, and the electron mobilities are 2000 $cm^2/V \cdot s$ and 2090 $cm^2/V \cdot s$ for QuanFINE and "Fe Buffer", respectively. These results indicate that the 2DEG properties are not affected by the device processing.

DC characteristics on HEMTs with the L_g of 200nm for both heterostructures show similar performance with a maximum drain current of ~1 A/mm and the peak transconductance of ~500 mS/mm (Fig 4.6). HEMTs on "Fe Buffer" show a slightly higher maximum current which might be due to higher electron mobility, higher n_s, and a lower R_c.

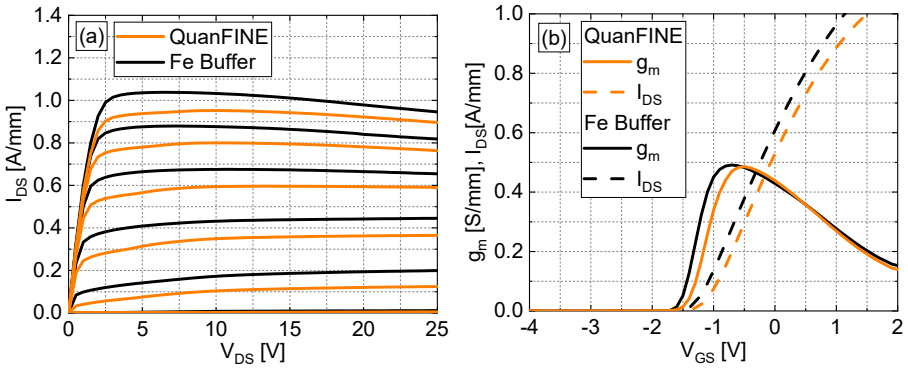

Figure 4.6. DC characteristics for HEMTs with an L_g of 200 nm on both materials. (a) I_{DS} versus V_{DS} for V_{GS} = -4:0.5:1 V, (b) shows I_{DS} and g_m versus V_{GS} for V_{DS} of 10 V [Paper C].

The breakdown voltage characterizations are performed on HEMTs with the L_g of 100 nm and 200 nm (Fig 4.7). HEMTs with the L_g of 200 nm on QuanFINE and "Fe Buffer" shows a catastrophic breakdown behaviour at ~80V (Fig 4.5 (a)(b)). Interestingly, QuanFINE presents a soft increase of the leakage current before a catastrophic breakdown, which might be due to a leakage path within the heterostructure or absence of acceptor-like Fe dopants to capture the electrons. The HEMTs with an L_g of 100 nm and a smaller gate-drain distance of 0.95 µm on QuanFINE also exhibits a soft breakdown behaviour (Fig 4.5 (d)). Further studies are required to understand the soft-breakdown mechanism.

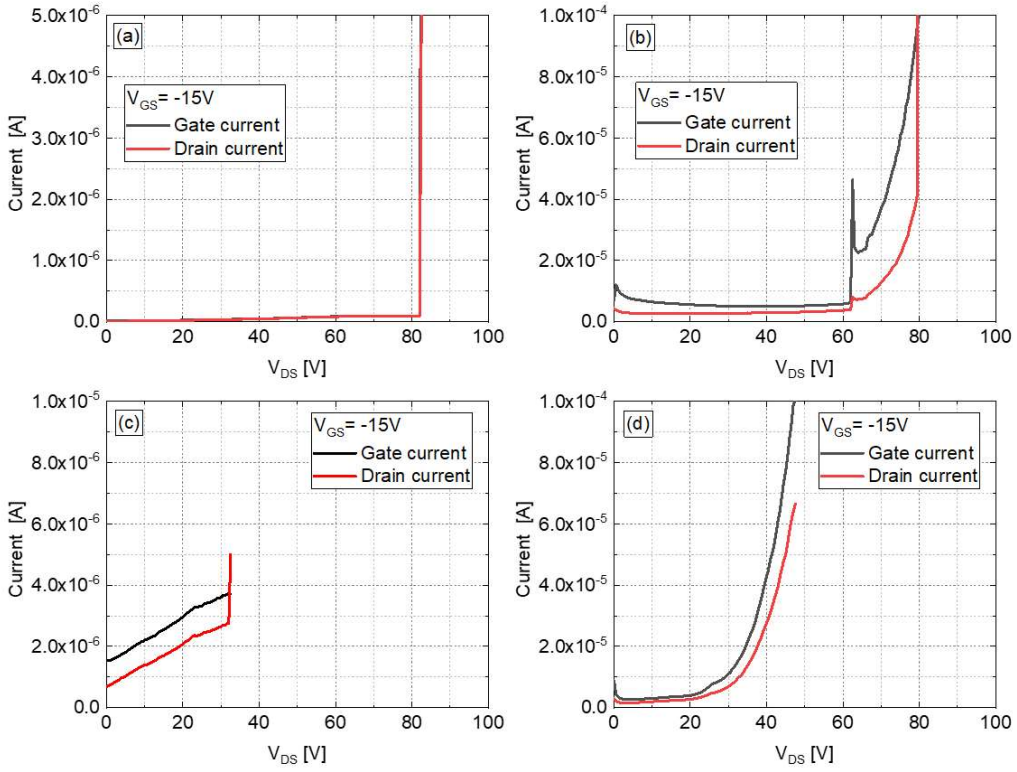

Figure 4.7. Break down characteristics on (a) "Fe Buffer" (L_g= 200 nm), (b) QuanFINE (L_g= 200 nm), (c) "Fe Buffer" (L_g= 100 nm), (d) QuanFINE (L_g= 100 nm) devices.

The short channel effects are characterized by drain induced barrier lowering (DIBL), defined as $|\Delta V_{TH}/\Delta V_{DS}|$ and subthreshold swing (SS) extracted from $\partial V_{GS}/\partial \log_{10}(I_{DS})$. DIBL was calculated using the pinch-off voltage (V_{po}), defined at I_{DS} of 1 mA/mm, at V_{DS} of 1 V, and 25 V. SS was calculated from the transfer characteristics as the minimum SS at V_{DS} = 10 V (Fig 4.8). HEMTs with a gate length of 200 nm on QuanFINE has a DIBL of ~13 mV/V, which is comparable to the DIBL of ~10 mV/V for the "Fe Buffer" material. The DIBL results are not in agreement with the TCAD simulations (Fig. 4.4) and further investigation is required to understand the discrepancy. Moreover, one order magnitude higher leakage current is revealed at the deep pinch-off condition for the HEMTs on QuanFINE, which might be due to the direct contact of gate and 2DEG at the mesa side-wall and the UID-GaN layer without Fe dopants. Besides, a subthreshold leakage is presented on QuanFINE at a V_{GS} of -2 V, which could also be due to the leakage paths within the heterostructure.

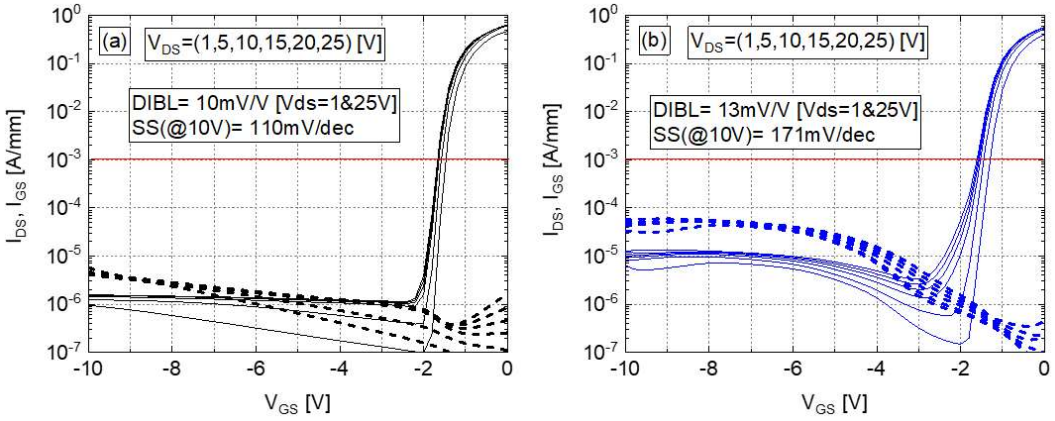

Figure 4.8. Short channel effects characteristics by DIBL and SS on HEMTs with the L_g of 200 nm, (a) "Fe Buffer" and (b) QuanFINE.

The pulsed-IV characteristics and the drain transient measurements are performed on HEMTs for both materials (Fig 4.9). QuanFINE shows a smaller current collapse and less dynamic R_{on} degradation than "Fe Buffer". Moreover, QuanFINE also exhibits a faster current recovery speed than "Fe Buffer" due to a pure UID-GaN layer which has less deep level traps. These results highlight the benefit of removing the Fe-doped GaN buffer, that inevitably leads to trapping effects.

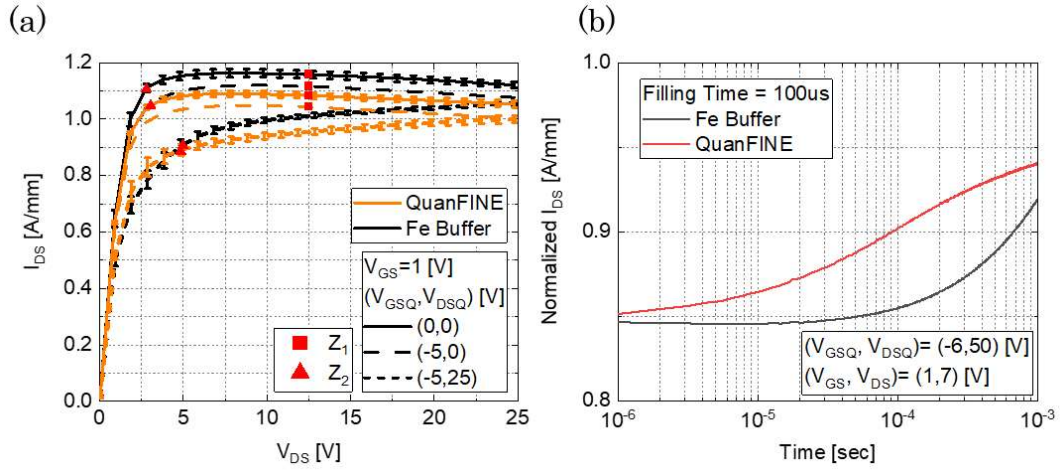

Figure 4.9. (a) Pulsed-IV measurements were performed at different quiescent biases. The results were extracted from 12 randomly selected HEMTs with L_g of 100 nm on QuanFINE and "Fe Buffer" samples [Paper A]. (b) Drain transient measurements on HEMTs with L_g of 200 nm on both heterostructures.

The load-pull measurements on HEMTs with a class-AB condition (~20% maximum drain current) are performed at 3 GHz with an active load-pull system [99]. The highest output power on both heterostructures is 4.1 W/mm with a similar efficiency of ~40 % at V_{DS} of 30 V (Fig 4.10). A similar large-signal performance is explained

by similar 2DEG confinement and breakdown voltage. Moreover, a higher drain current of "Fe Buffer" is compensated by lower gate-lag and drain-lag of QuanFINE, resulting in a similar knee voltage and knee current.

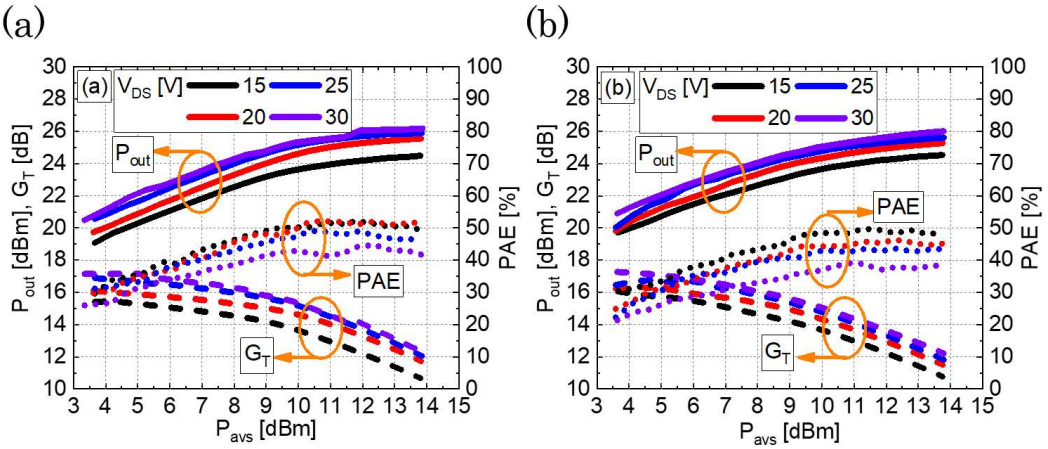

Figure 4.10. 3 GHz active load-pull measurements of HEMTs with an L_g of 200 nm performed at different drain bias on (a) "Fe Buffer" and (b) QuanFINE [Paper C].

Chapter 5

Conclusions and future work

The main aim of this work is to find an alternative method (QuanFINE) to suppress the short channel effects, minimize the buffer-related trapping effects, and reduce the thermal resistance of the epi-stack to improve the high-frequency performance of HEMTs. Moreover, the improvement of the HEMTs performance in general achieved by 1) reducing the surface-related traps by in-situ NH3 pretreatment before SiN passivation layer deposition and 2) reducing the contact resistivity loss by a deeply recessed low contact resistance Ta ohmic contacts are also presented in this work.

The deeply recessed gold-free Ta-based ohmic contacts are optimized, yielding a low contact resistance of 0.24 Ωmm achieved by a low annealing temperature of 575 °C. Low annealing temperature allows a sharp metal edge, benefiting the scaled-down of the device, i.e. reduce the source-gate distance for smaller gate length HEMTs. Due to the deeply recessed etching below the 2DEG, the contact metals are formed at the recessed sidewall. Therefore, it is less sensitive of the recessed etching depth than shallow recessed contact. Moreover, the issue of forming low contact resistance ohmic contacts on a high Al content barrier and AlN exclusion layer can be mitigated. Future work should focus on the in-situ ohmic process by in-situ plasma cleaning and sputter metal deposition to minimize the oxide layer between ohmic contacts and semiconductor. Besides, localized strain by SiN passivation influence the localized 2DEG properties, which has a strong impact on carrier tunneling possibility between ohmic contacts and the 2DEG channel. Further improvement of the contact resistance by introducing extra n-type doping is also favorable.

A plasma-free in-situ NH_3 pretreatment before LPCVD SiN deposition effectively reduces the DC-AC dispersion of HEMTs. A longer pretreatment duration reduces 40 % of the surface-related trapping effects as compared to that on the sample without the pretreatment. This improvement directly transfers to a better high-frequency performance with the output power of 3.3 W/mm, which is 26% higher than no pretreatment sample. Moreover, the on-wafer uniformity is also improved by the pretreatment. However, the sample with 10 min pretreatment still exhibits a small surface related current collapse. Future work should focus on improving the treatment methods on the surface of the epi-structure to achieve a trap-free surface. Moreover, the strain-induced 2DEG properties modification by LPCVD SiN should also be studied to further improve device performance.

A QuanFINE HEMT-structure with a thin 250 nm UID-GaN layer shows excellent DC performance with a saturation of 1 A/mm and peak transconductance of 500 mS/mm for HEMTs with the L_g of 100 nm. A good 2DEG confinement of QuanFINE is verified with the DIBL of 13 mV/V on the HEMTs with the L_g of 200 nm, resulting from the double heterostructure. Lower trapping effects on QuanFINE than conventional Fe-doped GaN buffer are confirmed due to the thin UID-GaN layer with a low level of impurities and structural defects. The RF performance of QuanFINE is comparable to a well-established Fe-doped buffer epi wafer. These results indicate huge potential of QuanFINE thanks to the removal of intentional dopants and utilizing band structure engineering to confine the 2DEG. Future work should focus on pushing the performance limit of QuanFINE. From the characteristics of the trapping effects, buffer related traps are revealed even in dopants-free QuanFINE. The origin of the buffer-related traps is to be investigated. Further reduction of UID-GaN layer thickness is critical for better confinement on small gate length devices. Different barrier designs including thin AlN and lattice match InAlN on QuanFINE requires further studies. The last but not the least, the device processing flows also require further upgrade and optimization to match the advanced Fe-free and buffer-free QuanFINE heterostructures.

Chapter 6

Summary of appended papers

This chapter summarizes the publications included in this work. The abstract and my contributions are presented for each publication.

Paper A

Y. K. Lin, J. Bergsten, H. Leong, A. Malmros, J. T. Chen, **D. Y. Chen**, O. Kordina, H. Zirath, E. Y. Chang and N. Rorsman, "A versatile low-resistance ohmic contact process with ohmic recess and low-temperature annealing for GaN HEMTs", *Semiconductor Science and Technology, vol. 33, iss. 9, pp. 095019, 2018.*

This publication investigates the deeply recessed gold-free Ta/Al/Ta ohmic contacts for III-N HEMTs technology. The low contact resistance of 0.24 Ωmm can be achieved when the metal stacks are deposited on the sidewall of the recess and annealed at 575 °C. This approach allows a less sensitive of recessed etching depth. Important parameters of the ohmic process include the metal coverage, slope angle of etching sidewall, bottom Ta-layer thickness, and annealing temperature and duration are studied. Moreover, these deeply recessed contacts are successfully implemented on different heterostructures with different AlGaN barrier thickness as well as with and without the AlN exclusion layer.

My contribution: YKL, JB, HL, AM, and DYC designed the experiments, fabricated the TLM structures, performed the measurements. YKL wrote the paper with feedback from the co-author.

Paper B

D. Y. Chen, K. H. Wen, M. Thorsell, O. Kordina, J. T. Chen, and N. Rorsman, "Impact of GaN HEMTs Performance by In-situ NH3 Pretreatment before LPCVD SiN_x Passivation", *Manuscript.*

This publication investigates the impact of GaN HEMTs high-frequency performance by in-situ plasma-free NH_3 pretreatment before the SiN passivation layer deposited by LPCVD. Time duration-dependent of in-situ NH_3 pretreatment is studied including 0, 3, and 10 mins pretreatment time duration. Longer pretreatment duration effectively reduces 40% of the surface-related trapping effects, resulting in better on-wafer uniformity and large signal performance with 27% higher output power and better efficiency.

My contribution: DYC designed the experiments, fabricated the HEMTs. DYC and KHW performed the measurements. DYC wrote the paper with feedback from the co-author.

Paper C

D. Y. Chen, A. Malmros, M. Thorsell, H. Hjelmgren, O. Kordina, J. T. Chen, and N. Rorsman, "Microwave Performance of 'Buffer-Free' GaN-on-SiC High Electron Mobility Transistors", *IEEE Electron Device Letters, vol. 41 , iss. 6 , 2020.*

This publication studies the high-frequency performance of the QuanFINE double-heterostructure AlGaN/UID-GaN/AlN on SiC, which has a thin UID-GaN layer with the thickness of 250 nm in between AlGaN barrier and the AlN nucleation layer. This approach allows the AlN nucleation layer to act as a back-barrier to confinement the 2DEG and minimize the buffer leakage current. The device is also benchmarked to conventional Fe-doped thick GaN buffer heterostructure with nominally the same barrier design from Cree. HEMTs with the Lg of 100 nm on QuanFINE shows similar DC performance with a saturation current of 1 A/mm and peak transconductance of 500 mS/mm as compared to Fe-doped material. Lower trapping effects are proven for the HEMTs on QuanFINE, which directly transfer to good high-frequency performance with the output power of 4.1 W/mm at 3 GHz.

My contribution: DYC designed the experiments, fabricated the HEMTs, and performed the measurements. AM supported the transistor model extraction. HH supported the TCAD simulation. DYC wrote the paper with feedback from the co-author.

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